Application No. 10/517,236
Filed: December 8, 2004
TC Art Unit: 2194
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REMARKS

Claims 1, 3-14 and 16-25 are pending in this application. Independent claim 1 has been amended to recite storing each event "in a first memory and a second memory," and that "the first memory and the second memory are associated with the management unit." In view of this amendment, claim 2 has been cancelled. Independent claim 13 has been amended to recite "a second memory internal to the management unit for storing the events in order to read them via the data bus." In view of this amendment, claim 15 has been cancelled.

The rejection of the method claims under § 101 is traversed on the grounds that these claims adequately recite the thing or product to which they are tied, for example, by identifying the apparatus that accomplishes the method steps. With respect to independent claim 1, the Examiner's attention is directed to the language specifying that "the above-mentioned management steps are carried out. . . by a management unit included in an independent management module connected to the data bus and incorporated into the standard computer system." It is thus clear that the present methods do not recite purely mental steps and are in fact tied to a particular apparatus. Reconsideration is respectfully requested.

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In the Office Action, independent claim 1 was rejected as being obvious over US 2003/0046324 to Sukuki *et al.* ("Suzuki") in combination with US 2002/0152185 to Jamadagni ("Jamadagni") and 4,538,235 to Henning ("Henning"). Independent claim 13 was rejected as being obvious over Suzuki, Jamadagni, Henning and US 2003/0197632 to Rubin *et al.* ("Rubin").

These rejections are respectfully traversed on the grounds that the differences between the claimed subject matter as a whole and the cited references are such that the present claims would not have been obvious to one of ordinary skill in the art.

As discussed in the previous Reply, the Suzuki reference teaches away from the present invention. Suzuki describes managing the execution order of a plurality of tasks in a programmable logic controller based on the classification of the tasks into different groups (i.e., communication task group, control task group, management task group). The controller 1 of Suzuki includes a single CPU 100 and an associated memory 17 that contains the programs that are executed by the CPU 100. The stated object of Suzuki's controller is to "guarantee[] both real-time execution of control processing and throughput of network communication processing by one information processing means." (See para. [0011]). Furthermore, Suzuki teaches "to execute both

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control processing and network communications processing in coexistence on one microprocessor and, basically, the number of microprocessors (CPU) on the controller is one." (See para. [0081]).

This is distinguishable from the method of managing events as recited in claim 1, which specifies that certain management steps are "carried out in real time *without access to the central unit* by a management unit included in an *independent management module* connected to the data bus and incorporated into the standard computer system." Suzuki is also distinguishable from independent claim 13, which recites "an independent management unit connected to the central unit via an interface and the data bus, said management unit being adapted to receive and process events in real time without intervention by the central unit." In fact, this is precisely the opposite of what is taught in Suzuki, in which all of the processing is performed by a single, central unit (CPU).

Independent claim 1 has also been amended by combining features of prior claims 2 and 6 to specify "storing each event in a first memory and a second memory," where the first memory and the second memory are associated with the management unit. Similarly, independent claim 13 has been amended to recite "a

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second memory internal to the management unit for storing the events in order to read them via the data bus." Contrary to the Examiner's assertions in the Office Action, Suzuki does not teach a management unit having a first memory and a second memory, as is presently recited. Suzuki describes a controller that has a single memory 17 associated with a CPU 100.

The secondary reference to Jamadagni is directed to correlating events in order to detect faults in a network system, which is a very different field from the event management methods and modules of the present claims, and is cited only for describing "events" as consisting of a time stamp, event type, event subtype, etc. Thus, as implicitly acknowledged by the Examiner, the combined teachings of Suzukia and Jamadagni do not render the present claims obvious.

Moreover, the present claims are still not rendered obvious by the addition of the newly-cited Henning reference. Henning does not disclose or remotely suggest the event management module or the even management steps as recited in the present claims. Henning describes "interval counter circuitry 84" that is connected to the central processing unit 12 by an internal data bus 50, 52. The interval counter circuitry 84 is configured to perform the limited function of retriggering a decrementing

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counter 88 whenever an external input signal is received, and to provide an interrupt signal to the central processing unit 12 when the counter 88 fully decrements before receiving the next external input signal.

Henning does not perform the event management steps of claim 1, including, for example, time-stamping and storing the received events, and assigning at least one appropriate action to each received event. Henning's interval counter circuitry 84 does not store any events at all, and certainly does not teach or suggest storing the received events in a first memory and a second memory associated with the management unit, as is presently recited. Similarly, with respect to claim 13, Henning does not describe or suggest a number of features of the present management module, including a time-stamping clock adapted to time-stamp the received events before storing them in a first memory internal to the management unit, a second memory internal to the management unit for storing the events in order to read them via the data bus; and a random-access memory containing a preprogrammed table of actions, associated with the management unit and adapted to assign appropriate actions to events received thereby.

Thus, even when the teachings of the primary Suzuki

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reference are combined with those of Jamadagni and Henning, the combination still would not provide the event management methods and modules defined by the present claims.

More significantly, as previously discussed, the primary Suzuki reference *teaches away* from an independent management module that carries out management steps without access to the central unit, as is presently claimed. Therefore, one skilled in the art would have no reason or motivation to incorporate Henning's interval counter circuitry with Suzuki's centralized processing scheme using a single processor, since Suzuki teaches away from such a modification.

The deficiencies with respect to the Suzuki, Jamadagni and Henning combination are also not overcome by any of the secondary references to Collins, Rubin, Cheriton, Sven and Sechi, which are each cited for disclosing specific features of the claims and do not otherwise appear relevant to the event management methods and modules of the present claims.

In view of the above amendments and remarks, it is believed that all rejections are overcome, and that the present application is allowable.

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The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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